IN THE CLAIMS:

1. (Original) A method for performing a wire-bonding operation in an integrated circuit, comprising the steps of:

measuring a plurality of bond distances within the integrated circuit, each corresponding to one of a plurality of wire bonds to be formed;

calculating an area under a hypothetical wire bond profile as a function of the plurality of bond distances, a baseline wire length, and a baseline loop height; and

bonding a wire across a given one of the bond distances to form a given one of the wire bonds;

the bonding step being configured to provide a wire bond profile for the given wire bond having an area thereunder that is substantially equal to the calculated area.

2. (Original) The method of claim 1, wherein the calculating step calculates the area under the hypothetical wire bond profile using an average of the plurality of bond distances.

3. (Original) The method of claim 1, wherein the area under the wire bond profile for the given wire bond is adjusted by adjusting a loop height of the given wire bond relative to the baseline loop height.

4. (Original) The method of claim 1, wherein the area under the wire bond profile for the given wire bond is adjusted by adjusting a wire length of the given wire bond relative to the baseline wire length.

5. (Original) The method of claim 1, wherein the calculating step comprises the step of calculating the area under the hypothetical wire bond profile using an integration technique.

6. (Original) The method of claim 1, wherein the bonding step comprises the step of calculating an area under a hypothetical wire bond profile for the given wire bond using the given bond distance, the baseline bond wire length, and the baseline loop height.

7. (Original) The method of claim 6, wherein the bonding step comprises comparing the area under the hypothetical wire bond profile for the given wire bond to the area calculated as a function of the plurality of bond distances.

8. (Original) The method of claim 1, wherein the area under the wire bond profile for the given wire bond is adjusted in conjunction with the bonding step if that area differs from the calculated area by more than a designated amount.

9. (Original) The method of claim 1, wherein the bonding step is repeated for each of the plurality of wire bonds to be formed.

10. (Original) The method of claim 1, wherein the bonding step comprises the step of bonding the wire between a die of the integrated circuit and a capacitor of the integrated circuit.

11. (Original) The method of claim 1, wherein the bonding step comprises the step of bonding the wire between a capacitor of the integrated circuit and a lead of a package of the integrated circuit.

12. (Original) The method of claim 1, wherein the bonding step comprises the step of bonding the wire between a die of the integrated circuit and a lead of a package of the integrated circuit.

13. (Original) The method of claim 1, wherein the bonding step comprises the step of bonding the wire to a bond pad.

14. (Original) The method of claim 1, wherein the bonding step comprises the step of bonding the wire to a bond strip.

15. (Original) The method of claim 1, wherein the integrated circuit comprises a radio frequency (RF) integrated circuit.

16. (Original) The method of claim 1, wherein the integrated circuit comprises a plurality of dies.

17. (Original) The method of claim 16, wherein the integrated circuit comprises a plurality of capacitors, one or more of the dies being disposed between a corresponding pair of the capacitors.

18-20. (Canceled)